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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,414	11/26/2003	Dustin P. Wood	P16830	2632

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EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 05/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/723,414	WOOD ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-13 and 16* is/are rejected.

7)☒ Claim(s) *14,15 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The present Office Action is responsive to Applicant's Amendment and Response filed February 07, 2006 (Certificate of Mailing date: February 02, 2006). The Examiner acknowledges the cancellation of Claims 1-10 and 18-27, and the amendment of base Claim 11. Accordingly, Claims 11-17 remain pending in the instant amended Application.

Rejections Based On Prior Art

2. The following references were relied upon for the rejections hereinbelow:

Tanahashi (US 6,184,477 B1) Broaddus et al. (US 4,916,260)†

†Already made of record by the Examiner in the previous Office Action of December 06, 2005.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 11 is rejected under 35 U.S.C. 102(b) as being anticipated by Tanahashi.

Tanahashi discloses, in Figs. 3 and 4: forming a first metal layer G1 on a first dielectric layer I1 (Fig. 4); forming a second dielectric layer I2 on the first metal layer G1 (Fig. 4); forming a second metal (signal) layer S1 on the second dielectric layer I2 (Fig.

4; col.11: 21-25); patterning the second metal layer S1 such that signal traces are formed in the second metal layer S1 (Fig. 3); patterning the first metal layer G1 as a substantially continuous sheet having slots (i.e., apertures defined by the grid lines) formed therein in a substantially rectangular pattern (Fig. 3) to allow the first and second dielectric layers I1 and I2 to adhere to each other by way of the slots (col.14: 66-col.15: 7); and adjusting an orientation of at least some of the slots in the substantially rectangular pattern such that none of the signal traces S1 passes over any of the slots (Fig. 3; col.11: 21-25 and 42-45).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 11-13 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Broaddus et al.

A) As to Claim 11:

I. Broaddus et al. discloses: forming a first metal layer 15 on a first dielectric layer 23 (Fig. 3; note that reference numeral "22" in Fig. 3 should be 23 instead); forming a second dielectric layer 21 on the first metal layer 15; forming a second metal layer S on the second, upper dielectric layer 21 (Fig. 10) as follows:

(i) Encapsulated circuit sheets 31 (Fig. 5) are formed as individual sheets that encapsulate the first metal layer 15, the first metal layer (and all other subsequent metal layers in the individual sheets 31) having slots 17 that allow dielectric layers 21 and 23 to adhere to each other by way of the slots and thereby form the plurality of encapsulated circuit sheets 31 (col.5: 64-col.6: 4).

(ii) These sheets are finally cured then separated (col.5: 33-42), then stacked again, using registration apertures 33 for alignment (col.6: 27-45 and 50-53), and then provided with still more slots 45, to completely electrically isolate the outer circuit portion from the inner circuit portion in first metal layer 15 (Fig. 9; col.7: 12-37), and further provided with clearance holes 41 for electrical interconnections (Figs. 8 and 9; col.6: 54-66).

(iii) Then these sheets 31 (now encapsulating first metal layer 15 are again separated from each other (col.7: 53-59). At this point, other

circuitry, such as patterned signal layers S and power layers P are formed on these encapsulated-circuit sheets 31 which, in their now-finished form are applied to the final product circuit, as shown in Fig. 10, wherein the numeral 61 represents the finished individual sheets 31 and a second metal layer S is formed and patterned with signal traces on the second (upper) dielectric layer 21 of the finished sheet 31 (Figs. 3 and 5), now referenced as sheet 61 in the final-product board of Fig. 10 (col.7: 53-col.8: 9). A portion of the final product circuit board is also shown in Fig. 11.

Patterning the first metal layer 15 as a substantially continuous sheet having slots 17 formed therein in a substantially rectangular pattern (Figs. 2 and 3) to allow the first and second dielectric layers 21 and 23 to adhere to each other by way of the slots 17 (Figs. 3 and 5; col.4: 18-23; col.5: 64-col.6: 4).

II. Broaddus et al. does not provide details that precisely locate the signal traces of the second metal (signal) layer S on the second dielectric layer 21 of the sheet 61 in Fig. 10 (that represents the finished sheet 31 of Figs. 3 and 5).

III. However, since the slots 17, in conjunction with slots 45, completely electrically isolate the outer (peripheral) portion of first metal layer 15 from its inner--interior--portion (Fig. 9; col.7: 12-27), slots 17 and 45 forming the dividing line between the active inner circuit portion and the electrically isolated--hence, non-functional--outer peripheral portion, then it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the orientation of at least some of slots 17 in

the substantially rectangular pattern--that define, along with slots 45, the border line between the active interior portion and the non-functional peripheral portion of first metal layer 15--such that none of the signal traces--of second metal (signal) layer S on dielectric layer 21 of sheet 61--passes over any of the slots 17 since that outer, peripheral portion of the circuit is an electrically isolated, hence, non-functional region, its primary reason-for-being only to provide the mechanically secure and reliable lamination of the multiple circuit layers of the multilayer board of Figs. 10 and 11 by way of slots 17, and therefore not requiring any of the signal traces to cross over the bordering slots 17 from the electrically active interior region of the circuit to the isolated non-functional peripheral portion to be electrically connected to the electrically non-functional peripheral portion.

B) As to Claim 12, Broaddus et al. further discloses each of the slots 17 has a length:width ratio of at least 5:1 (col.4: 30-33 teaches an aspect ratio of 2":0.125" = 16:1).

C) As to Claim 13, Broaddus et al. further discloses each of the slots 17 has a length:width ratio of at least 10:1 (col.4: 30-33 teaches an aspect ratio of 2":0.125" = 16:1).

D) As to Claim 16, Broaddus et al. further discloses, in Fig. 2, a first one of slots 17 (say, the vertical slot 17 near the upper left corner of the rectangular array) has an orientation that is at an angle (a right-angle) relative to an orientation of a second one of the slots 17 (i.e., the horizontal slot 17 that is adjacent to the vertical slot 17).

Allowable Subject Matter

8. Claims 14-15 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

9. Applicant's arguments, see pp.4-5 of instant Amendment and Response, filed February 07, 2006, with respect to the rejections of Claims 11-14 and 16 under 35 USC § 102(b) have been fully considered and are persuasive due to Applicant's amendment of base Claim 11 over Takahashi et al. (US 6,106,923). Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly found prior art. The rejections have been set forth, above.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

A) Koga et al. (US 6,426,469 B2) discloses, in Figs. 3 and 4: forming a first metal layer 2 on a first dielectric layer 100; forming a second dielectric layer 4 on the first metal layer 2; forming a second metal layer on the second dielectric layer 4; patterning the second metal layer such that signal traces 1 and 6 are formed in the second metal layer; patterning the first metal layer 2 as a substantially continuous sheet having slots 12 and 16 formed therein to allow the first and second dielectric layers to adhere to

each other by way of slots 12 and 16 (col.5: 3-10 and 43-53); and adjusting an orientation of at least some of the slots 12 and 16 such that none of the signal traces 1 and 6 passes over any of slots 12 and 16 (col.5: 37-41 and 53-56). Koga et al. does not teach that the continuous metal layer sheet 2 has slots 12 and 16 formed therein in a substantially rectangular pattern.

B) Govind et al. (US 6,496,081 B1) discloses a circuit board with slot apertures oriented such that differential pair traces pass over the slots (Figs. 2 and 3). Alternatively, the traces may be entirely between the slots. Also, the slots may have any of a number of shapes (col.3: 59-col.4: 3). The purpose of the slots is to improve signal integrity along differential pair traces.

C) Mazumder (US 6,191,472 B1) discloses a circuit board with slots 128 for collecting gas during the heating of the polyimide layers during testing and also for improving electrical performance of the IC components mounted on the circuit board (col.4: 20-27; col.5: 1-24). The slots 128 are oriented such that none of the traces 122A-E pass over any of the slots 128 (Fig. 6; col.5: 31-48).

D) Waizman et al. (US 6,392,301 B1) discloses, in Fig. 6, a conductive layer 400 and signal traces 510 separated by at least one layer of dielectric material (col. 5: 60-63), slots 412, 414, 416 and 418 oriented conductive layer 400 such that traces 510 do not pass over any of the slots (col.6: 32-48 and 63-67). The slots are used for degassing and also reducing the variation in characteristic impedance from trace to trace (col.6: 49-51; col.6: 63-col.7: 2).

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
April 30, 2006